CHAPTER 4: Capacitance Model

Previous BSIM capacitance models used long channel charge models in which the ratio of C_{ij}/L_{eff} (where i and j are the transistor nodes) did not scale with L_{eff}. This resulted in an overestimation of capacitance values for devices smaller than a L_{drawn} of 2 μm. This effect was particularly severe at low drain biases. In addition, previous capacitance models also showed appalling discontinuities for the gate capacitance at threshold voltage. These factors as wells as others necessitated the development of a new charge and capacitance model.

4.1 General Information

In BSIM3v3, a new capacitance formulation addresses the above concerns. This new model incorporates the following enhancements:

- Separate effective channel length and width are used for capacitance and I-V models.
- A simple short channel capacitance model with accuracy down to the 0.2 μm Leff range.
- Intrinsic C-V model is no longer piece-wise (i.e. divided into inversion, depletion, triode and saturation regions). Instead, a single equation is used for each nodal charge covering all regions of operation. This ensures continuity of all derivatives and enhances convergence properties. The inversion

capacitance and substrate capacitance are also no longer discontinuous at the threshold voltage.

- Threshold voltage formulation is consistent with the I-V model. Effects such as body effect and DIBL are automatically incorporated in the capacitance model.
- Overlap capacitance comprises two parts: 1) a bias independent part which models the effective overlap capacitance between the gate and the heavily doped source/drain, and 2) a gate bias dependent part between the gate and the lightly doped source/drain region.
- Bias independent, fringing capacitances are added between the gate and source as well as the gate and drain.

To accommodate these changes, new parameters are introduced (Table 4-1).

Name	Function	Default	Unit
CAPMOD	Flag for short channel capacitance model	2	(True)
CGS1	Lightly-doped source to gate overlap capacitance	0	(F/m)
CGD1	Lightly-doped drain to gate overlap capacitance	0	(F/m)
CKAPPA	Coefficient for lightly-doped overlap capacitance	0.6	
CF	Fringing field capacitance	equation (4.4.2)	(F/m)
CLC	Constant term for short channel model	0.1	μm
CLE	Exponential term for short channel model	0.6	
DWC	Long channel gate capacitance width offset	Wint	μm
DLC	Long channel gate capacitance length offset	Lint	μm

Table 4-1. New parameters for BSIM3v3 capacitance model.

4.2 A Note on Device Geometry Dependencies

For capacitance modeling considerations, a transistor can be divided into 2 regions: intrinsic and extrinsic. The **intrinsic** part is the region between the metallurgical source and drain junction when the gate to S/D region is at flat band voltage. The **extrinsic** part, basically the parasitics, is further divided into three regions: 1) the outer fringing capacitance between the polysilicon gate and the source/drain, 2) the overlap between the gate and the heavily doped S/D region (relatively insensitive to bias conditions), and 3) the overlap between the gate and lightly doped S/D region which changes with bias.

In the previous C-V model (BSIM3 Version 2.0), both the I-V and C-V parts of the model used the same Leff and Weff expressions.. This is not so in the new model BSIM3v3. The geometry dependence for the **intrinsic** capacitance part is given as the following:

$$\delta W_{eff} = DWC + \frac{Wl}{L^{\mathrm{Wln}}} + \frac{Ww}{W^{Wwn}} + \frac{Wwl}{L^{Wln} W^{Wwn}} \tag{4.2.1}$$

$$\delta L_{eff} = DLC + \frac{Ll}{L^{Lln}} + \frac{Lw}{W^{Lwn}} + \frac{Lwl}{L^{Lln} W^{Lwn}} \tag{4.2.2}$$

$$L_{active} = L_{drawn} - 2\delta L_{eff} \tag{4.2.3}$$

$$W_{active} = W_{drawn} - 2\delta W_{eff} \tag{4.2.4}$$

The meanings of *DWC* and *DLC* are different from those of *Wint* and *Lint* in the I-V model. L_{active} and W_{active} are the effective length and width of the intrinsic

device for capacitance calculations. Unlike the case with I-V, we assumed that these dimensions have no voltage bias dependence. The parameter δLeff is equal to the source/drain to gate overlap length plus the difference between drawn and actual POLY CD due to processing (gate printing, etching and oxidation) on one side. Overall, a distinction should be made between the effective channel length extracted from the capacitance measurement and from the I-V measurement.

Traditionally, the Leff extracted during I-V model characterization is used to gauge a technology. However this Leff does not necessarily carry a physical meaning. It is just a parameter used in the I-V formulation so that the measured I-V characteristics match those calculated by the model. This Leff is therefore very sensitive to the I-V equations used and also to the conduction characteristics of the LDD region relative to the channel region. A device with a large Leff and a small parasitic resistance can have a similar current drive as another with a smaller Leff but larger R_{ds}. In some cases Leff can be larger than the polysilicon gate length giving Leff a dubious physical meaning (negative Leff).

The L_{active} parameter extracted from the capacitance method is a closer representation of the metallurgical junction length (physical length). Due to the graded source/ drain junction profile the source to drain length can have a very strong bias dependence. We therefore define L_{active} to be that measured at gate to source/drain flat band voltage. If the values for *DWC* and *DLC* are not specified in the SPICE model card, BSIM3v3's capacitance model will assume that the device in question has the same effective dimensions for both I-V and C-V models (i.e. *DWC = Wint* and *DLC=Lint).*

4.3 Intrinsic Capacitance

4.3.1 Background Information

There has been no recent major work performed in the area of intrinsic capacitance modeling suitable for implementation into a circuit simulator. One bottleneck is the difficulty in capacitance measurement, especially in the deep micron regime. At very short channel lengths, the MOSFET intrinsic capacitance is very small yet the conductance is large. The large conductance results in large in-phase currents during high frequency measurement and overloads the C-V meter. Also the effects of the parasitic inductance in the experimental setup will be more profound. Moreover, since charge can only be measured at high impedance nodes (i.e. the gate and substrate nodes), only 8 of the 16 capacitance components in an intrinsic MOSFET, can be directly measured.

An alternative solution is to use a 2-D device simulator such as PISCES. However, the simulation results are not always satisfactory. Another reason for the lack of development work is the observation that most circuits used to be dominated by interconnect and junction capacitances. An exact model for the intrinsic transistor capacitance is of lesser importance. However, this may no longer be true with the continuous shrinking of design rules. Also, a well behave capacitance model will help circuit simulation convergence. In low power and analog applications, designers are interested in device operation near threshold voltage. Thus, the model must also be accurate in transition regions as well. To ensure proper behavior, both the I-V and C-V model equations should be

developed from an identical set of charge equations so that C_{ij}/I_d is well behaved.

Similar to the I-V model, the development of the capacitance model was carried out with an effort to balance physics with simulation efficiency. Several physical models have been published. These were either too complicated or lacked continuity from one operation region to another. A good model should be simple yet include most of the physical concepts.

4.3.2 Basic Formulation

To ensure charge conservation, terminal charges instead of the terminal voltages are used as state variables. The terminal charges Q_g, Q_b, Q_s, and Q_d are the charges associated with the gate, bulk, source, and drain, respectively. The gate charge is comprised of mirror charges from 3 components: the channel minority (inversion) charge (Q_{inv}), the channel majority (accumulation) charge (Q_{acc}) and the substrate fix charge (Q_{sub}).

The accumulation charge and the substrate charge are associated with the substrate node while the channel charge comes from the source and drain nodes:

(4.3.1)

$$\begin{cases} Q_g = -\left(Q_{sub} + Q_{inv} + Q_{acc}\right) \\ Q_b = Q_{acc} + Q_{sub} \\ Q_{inv} = Q_s + Q_d \end{cases}$$

The substrate charge can be divided into two components - the substrate charge at zero source-drain bias (Q_{sub0}), which is a function of gate to

substrate bias, and the additional non-uniform substrate charge in the presence of a drain bias (δQ_{sub}). Q_g now becomes:

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + \delta Q_{sub}\right) \tag{4.3.2}$$

The total charge is computed by integrating the charge along the channel. The threshold voltage along the channel is modified due to the non-uniform substrate charge by:

$$V_{th}(y) = V_{th}(0) + (A_{bulk} - 1)V_y \tag{4.3.3}$$

(4.3.4)

$$\text{therefore} \quad \begin{cases} Q_c = W_{active} \int_0^{L_{active}} q_c dy = W_{active} C_{ox} \int_0^{L_{active}} \left(V_{gt} - A_{bulk} V_y\right) dy \\ Q_g = W_{active} \int_0^{L_{active}} q_g dy = W_{active} C_{ox} \int_0^{L_{active}} \left(V_{gt} + V_{th} - V_{FB} - \phi_s - V_y\right) dy \\ Q_b = W_{active} \int_0^{L_{active}} q_b dy = -W_{active} C_{ox} \int_0^{L_{active}} \left(V_{th} - V_{FB} - \phi_s - (1 - A_{bulk}) V_y\right) dy \end{cases}$$

Substituting the following:

$$dy = \frac{dV_y}{\varepsilon_y}$$

and

$$J_{ds} = \frac{\mu_{eff} C_{ox}}{L_{active}} \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds}\right) V_{ds} = \mu_{eff} C_{ox} \left(V_{gt} - A_{bulk} V_{ds}\right) \varepsilon_y \tag{4.3.5}$$

into Eq. (4.3.4), we have the following upon integration:

(4.3.6)

$$\begin{cases} Q_c = -W_{active} L_{active} C_{ox} \left(\left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right) + \frac{A_{bulk}^{\ 2} V_{ds}^{\ 2}}{12 \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right)} \right) \\ Q_b = -Q_g - Q_c = Q_{sub0} + \delta Q_{sub} \\ Q_g = -Q_{sub0} + W_{active} L_{active} C_{ox} \left(\left(V_{gt} - \frac{V_{ds}}{2} \right) + \frac{A_{bulk} V_{ds}^{\ 2}}{12 \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right)} \right) \end{cases}$$

where,

(4.3.7)

$$\begin{cases} Q_{sub0} = -W_{active} L_{active} \sqrt{2 \varepsilon_{Si} q N_b \left(2 \phi_b - V_{bs} \right)} \\ \delta Q_{sub} = W_{active} L_{active} C_{ox} \left(\frac{1 - A_{bulk}}{2} V_{ds} - \frac{\left(1 - A_{bulk} \right) A_{bulk} V_{ds}^{\ 2}}{12 \left(V_{active} - \frac{A_{bulk}}{2} V_{ds} \right)} \right) \end{cases}$$

The inversion charges are supplied from the source and drain electrodes such that $Q_{inv} = Q_s + Q_d$. The ratio of Q_d and Q_s is the charge partitioning ratio. Existing charge partitioning schemes are 0/100, 50/50 and 40/60 (*XPART* = 0, 0.5 and 1) which are the ratios of Q_d to Q_s in the saturation region. We will revisit charge partitioning in Section 4.3.4.

All capacitances are derived from the charges to ensure charge conservation. Since there are 4 nodes, there are altogether 16 components. For each component:

(4.3.8)

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

where i and j denote transistor nodes. In addition:

$$\sum_i C_{ij} = \sum_j C_{ij} = 0$$

4.3.3 Short Channel Model

In deriving the long channel charge model, mobility is assumed to be constant with no velocity saturation. Therefore in the saturation region ($V_{ds} \geq V_{dsat}$), the carrier density at the drain end is zero. Since no channel length modulation is assumed, the channel charge will remain a constant throughout the saturation region. In essence, the channel charge in the saturation region is assumed to be zero. This is a good approximation for long channel devices but fails when $L_{eff} < 2$ μm. If we define a drain bias, $V_{dsat,cv}$, in which the channel charge becomes a constant, we will find that $V_{dsat,cv}$ in general is larger than V_{dsat} but smaller than the long channel V_{dsat}, given by V_{gt}/A_{bulk} (A_{bulk} is a parameter modeling the non-uniform substrate charge). However, in the old long channel charge model $V_{dsat,cv}$ is set to V_{gt}/A_{bulk} independent of channel length. Consequently, C_{ij}/Leff also has no channel length dependence (Eqs. (4.3.6), (4.37)). A pseudo short channel modification from the long channel has been used in the past. It involved the parameter A_{bulk} in the capacitance model which was redefined to be equal to V_{gt}/V_{dsat}, thereby equating $V_{dsat,cv}$ and V_{dsat}. This

overestimated the effect of velocity saturation and resulted in a smaller channel capacitance.

The difficulty in developing a short channel model lies in calculating the charge in the saturation region. Although current continuity stipulates that the charge density in the saturation region is almost constant, it is difficult to calculate accurately the length of the saturation region. Moreover, due to the exponentially increasing lateral electric field, most of the charge in the saturation region are not controlled by the gate electrode. However, one would expect that the total charge in the channel will exponentially decrease with drain bias. A physical model has been developed to reflect this but will not be presented here. A simpler model is adopted to empirically fit $V_{dsat,cv}$ to channel length. Experimentally,

(4.3.9)

$$V_{dsat,iv} < V_{dsat,cv} < V_{dsat,iv}\Big|_{L_{active}\to\infty} = \frac{V_{gsteff,cv}}{A_{bulk}}$$

and Vdsat,cv is fitted empirically by the following:

(4.3.10a)

$$V_{dsat,cv} = \frac{V_{gsteff,cv}}{A_{bulk}\left(1+\left(\frac{CLC}{L_{active}}\right)^{CLE}\right)}$$

(4.3.10b)

$$V_{gsteff,cv} = nv_t \ln\left(1+\exp\left(\frac{V_{gs}-V_{th}}{nv_t}\right)\right)$$

The parameter A_{bulk} can now be substituted by A_{bulk}' in the long channel equation where:

$$A_{bulk}' = A_{bulk0}\left(1+\left(\frac{\mathrm{CLC}}{L_{active}}\right)^{\mathrm{CLE}}\right) \tag{4.3.11}$$

$$A_{bulk0} = \left(1+\frac{K_1}{2\sqrt{\Phi_s - V_{bseff}}}\left\{\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{X_J X_{dep}}}+\frac{B_o}{W_{eff}'+B_1}\right\}\right)\frac{1}{1+K_{ETA}V_{bseff}} \tag{4.3.11a}$$

By setting *CLC* to zero, the new model reduces back to the old model. At very short channel lengths where velocity overshoot is prominent, the channel charges is only a weak function of channel length and saturation velocity. The effect of velocity overshoot is minimal and is not implemented into the model.

4.3.4 New Single Equation Formulation

In the old formulation, the capacitance is divided into four regions. There were separate equations modeling the nodal charges in each region. From one region to another the charges were conserved, but not their slopes. Therefore, the capacitances in some of these transitions were discontinuous. In the new model, a single equation is used to model each charge for all regions.

(a) Transition from depletion to inversion region

The biggest discontinuity is the inversion capacitance at threshold voltage. The old model uses a step function and the inversion capacitance changes

abruptly from 0 to C_{ox}. Concurrently, since the substrate charge is a constant, the substrate capacitance drops abruptly to 0 at threshold voltage. Both of these effects cause oscillation during circuit simulation. Experimentally, capacitance starts to increase almost quadratically at ~0.2V below threshold voltage and levels off at ~0.3V above threshold voltage. For analog and low power circuits, an accurate capacitance model around the threshold voltage is very important.

The non-abrupt channel inversion capacitance and substrate capacitance model is developed from the new I-V model which uses a single equation to formulate the subthreshold, transition and inversion regions. The new channel inversion charge model can be modified to any charge model by substituting V_{gt} with $V_{gsteff,cv}$ as in the following:

$$Q_{(inv,s,d)}(V_{gt}) = Q_{(inv,s,d)}(V_{gsteff,cv}) \tag{4.3.12}$$

Now,

$$\begin{cases} C_{(inv,s,d),g}(V_{gt}) = C_{(inv,s,d),g}(V_{gsteff,cv})\dfrac{\partial V_{gxt}}{\partial V_{gs}} \\ C_{(inv,s,d),(s,d,b)}(V_{gt}) = C_{(inv,s,d),(s,d,b)}(V_{gsteff,cv}) \end{cases} \tag{4.3.13}$$

where,

(4.3.14)

$$\frac{\partial V_{gsteff,cv}}{\partial V_{gs}} = \frac{\exp\left(\frac{V_{gst}}{nv_t}\right)}{\left(1 + \exp\left(\frac{V_{gst}}{nv_t}\right)\right)}$$

The "inversion" (minority) charge is always non-zero, even in the accumulation region. However, it decreases exponentially with gate bias in the subthreshold region.

(b) Transition from accumulation to depletion region

A parameter VFBeff is used to smooth out the transition between accumulation and depletion regions. It affects the accumulation and depletion charges:

(4.3.16)

$$V_{FBeff} = vfb - 0.5\left\{V_3 + \sqrt{V_3^{\,2} + 4\delta_3 vfb}\right\} \quad where \quad V_3 = vfb - V_{gb} - \delta_3; \quad \delta_3 = 0.02$$

(4.3.16a)

$$vfb = V_{th} - \phi_s - K_1\sqrt{\phi_s}$$

(4.3.17)

$$Q_{acc} = -W_{active} L_{active} C_{ox} \left(V_{FBeff} - vfb\right)$$

(4.3.18)

$$Q_{sub0} = -W_{active} L_{active} C_{ox} \frac{K_1^{\,2}}{2} \left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - V_{FBeff} - V_{gsteff\,cv} - V_{bseff}\right)}{K_1^{\,2}}}\right)$$

(c) Transition from linear to saturation region

A parameter Vcveff is used to smooth out the transition between linear and saturation regions. It affects the inversion charge.

(4.3.19)

$$V_{cveff} = V_{dsat,cv} - 0.5\left\{V_4 + \sqrt{V_4^{\,2} + 4\delta_4 V_{dsat,\,cv}}\right\} \quad where \quad V_4 = V_{dsat,cv} - V_{ds} - \delta_4; \quad \delta_4 = 0.02$$

(4.3.20)

$$Q_{inv} = -W_{active} L_{active} C_{ox} \left(\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right) + \frac{A_{bulk}'^{\,2} V_{cveff}^{\,2}}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

Below is a list of all he three partitioning schemes for the inversion charge:

(4.3.21)

$$\delta Q_{sub} = W_{active} L_{active} C_{ox} \left(\frac{1 - A_{bulk}'}{2} V_{cveff} - \frac{(1 - A_{bulk}') A_{bulk}' V_{cveff}^{\,2}}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff} \right)} \right)$$

(i) The 50/50 Charge partition

This is the simplest of all partitioning schemes in which the inversion charges are assumed to be contributed equally from the source and drain nodes. Despite it's simplicity it is found to approximate the simulation data well.

(4.3.22)

$$Q_s = Q_d = 0.5Q_{inv} = -\frac{W_{active}L_{active}C_{ox}}{2}\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2}V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{12\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2}V_{cveff}\right)}\right)$$

(ii) The 40/60 Channel-charge Partition

This is the most physical model of the three partitioning schemes in which the channel charges are allocated to the source and drain electrodes by assuming a linear dependence to the distance.

(4.3.23)

$$\begin{cases} Q_s = W_{active}\int_0^{L_{active}} q_c\left(1 - \frac{y}{L_{active}}\right)dy \\ Q_d = W_{active}\int_0^{L_{active}} q_c\frac{y}{L_{active}}dy \end{cases}$$

(4.3.24)

$$Q_s = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteff\,cv} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffcv}^3 - \frac{4}{3}V_{gstefcvf}^2\left(A_{bulk}'V_{cveff}\right) + \frac{2}{3}V_{gsteff}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

(4.3.25)

$$Q_d = -\frac{W_{active}L_{active}C_{ox}}{2\left(V_{gsteffcv} - \frac{A_{bulk}'}{2}V_{cveff}\right)^2}\left(V_{gsteffcv}^3 - \frac{5}{3}V_{gsteff\,cv}^2\left(A_{bulk}'V_{cveff}\right) + V_{gsteff\,cv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3\right)$$

(iii) The 0/100 Charge Partition

In fast transient simulations, the use of a quasi-static model may result in a large unrealistic drain current spike. This partitioning scheme is developed to artificially suppress the drain current spike by assigning all inversion charges in the saturation region to the source electrode. Notice that this charge partitioning scheme will still give drain current spikes in the linear region and aggravate the source current spike problem.

$$Q_s = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteff,cv}}{2} + \frac{A_{bulk}' V_{cveff}}{4} - \frac{\left(A_{bulk}' V_{cveff}\right)^2}{24\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff}\right)} \right) \tag{4.3.26}$$

$$Q_d = -W_{active} L_{active} C_{ox} \left(\frac{V_{gsteff,cv}}{2} - \frac{3A_{bulk}' V_{cveff}}{4} + \frac{\left(A_{bulk}' V_{cveff}\right)^2}{8\left(V_{gsteff,cv} - \frac{A_{bulk}'}{2} V_{cveff}\right)} \right) \tag{4.3.27}$$

(d) Bias dependent threshold voltage effects on capacitance

The effects of body bias and DIBL is included in the capacitance model by modifying the threshold voltage to make it consistent with the I-V model. In deriving the capacitances additional differentiations are need to account for the dependence of threshold voltage on drain and substrate biases. The intrinsic capacitances can be derived based on the above charge equations.

(4.3.28)

$$C_{(s,d,g,b),g} = \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}}$$

(4.3.29)

$$C_{(s,d,g,b),s} = -\frac{\partial Q_{s,d,g,b}}{\partial V_{ds}} + \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteffcv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \left(\frac{\partial V_{th}}{\partial V_{ds}} + \frac{\partial V_{th}}{\partial V_{bs}} \right)$$

(4.3.30)

$$C_{(s,d,g,b),d} = \frac{\partial Q_{s,d,g,b}}{\partial V_{ds}} - \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteff}cv} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{ds}}$$

(4.3.31)

$$C_{(s,d,g,b),b} = \frac{\partial Q_{s,d,g,b}}{\partial V_{bs}} - \frac{\partial Q_{s,d,g,b}}{\partial V_{gsteff}{}^{cv}} \frac{\partial V_{gsteffcv}}{\partial V_{gt}} \frac{\partial V_{th}}{\partial V_{bs}}$$

4.4 Extrinsic Capacitance: Fringing Capacitance

The fringing capacitance consists of a bias independent outer fringing capacitance and a bias dependent inner fringing capacitance. In the present release only the bias independent outer fringing capacitance is implemented. Experimentally, it is virtually impossible to separate this capacitance with the overlap capacitance. Nonetheless, the outer fringing capacitance can be theoretically calculated:

(4.4.1)

$$CF = \frac{\varepsilon_{ox}}{\alpha} ln\left(1 + \frac{t_{poly}}{t_{ox}}\right) \qquad \alpha = \frac{\pi}{2}$$

If *CF* is not given in the above expression, it can be calculated by:

(4.4.2)

$$CF = \frac{2\varepsilon_{ox}}{\pi} ln\left(1 + \frac{4 \times 10^{-7}}{t_{ox}}\right)$$

4.5 Extrinsic Capacitance: Overlap Capacitance

An accurate model for the overlap capacitance is essential. This is especially true for the drain side where the effect of the capacitance is amplified by the transistor gain. In old capacitance models this capacitance is assumed to be bias independent. However, experimental data show that the overlap capacitance changes with gate to source and gate to drain biases. In a single drain structure or the heavily doped S/D to gate overlap region in a LDD structure the bias dependence is the result of depleting the surface of the source and drain regions. Since the modulation is expected to be very small we can model this region with a constant capacitance. However in LDD MOSFETs a substantial portion of the LDD region can be depleted, both in the vertical and lateral directions. This can lead to a large reduction of overlap capacitance. This LDD region can be in accumulation or depletion. We use a single equation for both regions by using such smoothing parameters as $V_{gs,overlap}$ and $V_{gd,overlap}$ for the source and drain side, respectively. Unlike the case with the intrinsic capacitance, the overlap capacitances are reciprocal. In other words, $C_{gs,overlap} = C_{sg,overlap}$ and $C_{gd,overlap} = C_{dg,overlap}$.

(a) Source Overlap Charge

(4.5.1)

$$\frac{Q_{overlap,s}}{W_{active}} = \text{CGS0}V_{gs} + \text{CGS1}\left\{V_{gs} - V_{gs,overlap} + \frac{\text{CKAPPA}}{2}\left(-1 + \sqrt{1 + \frac{4V_{gs,overlap}}{\text{CKAPPA}}}\right)\right\}$$

(4.5.2)

$$V_{gs,overlap} = \frac{1}{2}\left\{\left(V_{gs} - \delta_1\right) + \sqrt{\left(V_{gs} - \delta_1\right)^2 - 4\delta_1}\right\} \quad where \quad \delta_1 = 0.02$$

where *CKAPPA* is a user input parameter. If the average doping in the LDD region is known, *CKAPPA* can be calculated by:

$$\frac{2e_{Si}qN_{LDD}}{C_{ox}^{\ 2}}$$

The typical value for N_{LDD} is 5x1017 cm-3.

(b) Drain Overlap Charge

(4.5.3)

$$\frac{Q_{overlap,d}}{W_{active}} = \text{CGD0}V_{gd} + \text{CGD1}\left\{V_{gd} - V_{gd,overlap} + \frac{\text{CKAPPA}}{2}\left(-1 + \sqrt{1 + \frac{4V_{gd,overlap}}{\text{CKAPPA}}}\right)\right\}$$

(4.5.4)

$$V_{gd,overlap} = \frac{1}{2}\left\{\left(V_{gd} - \delta_2\right) + \sqrt{\left(V_{gd} - \delta_2\right)^2 - 4\delta_2}\right\} \quad where \quad \delta_2 = 0.02$$

(c) Gate Overlap Charge

(4.5.5)

$$Q_{overlap,g} = -\left(Q_{overlap,s} + Q_{overlap,d}\right)$$

In the above expressions, if *CGS0* and *CGD0* (the heavily doped S/D region to gate overlap capacitance) are not given, they are calculated according to the following:

CGS0 = (*DLC*Cox)* - *CGS1* (if *DLC* is given and *DLC* > *0*)

CGS0 = 0 (if the previously calculated *CGS0* is less than 0)

CGS0 = 0.6 *Xj*Cox* (otherwise)

CGD0 = (*DLC*Cox)* - *CGD1* (if *DLC* is given and *DLC* > *CGD1/Cox*)

CGD0 = 0 (if previously calculated *CDG0* is less than 0)

CGD0 = 0.6 *Xj*Cox* (otherwise)

4.6 Graphical Results

Figures 4-1 through 4-4 are included to show the good behavior of the expressions introduced in this chapter. Note that both capacitance and charge are continuous under both Vds bias ranges (linear to saturation) and Vgs bias conditions (subthreshold to strong inversion). Figure 4-5 is also included to highlight the VFBeff equation used to ensured this continuity.

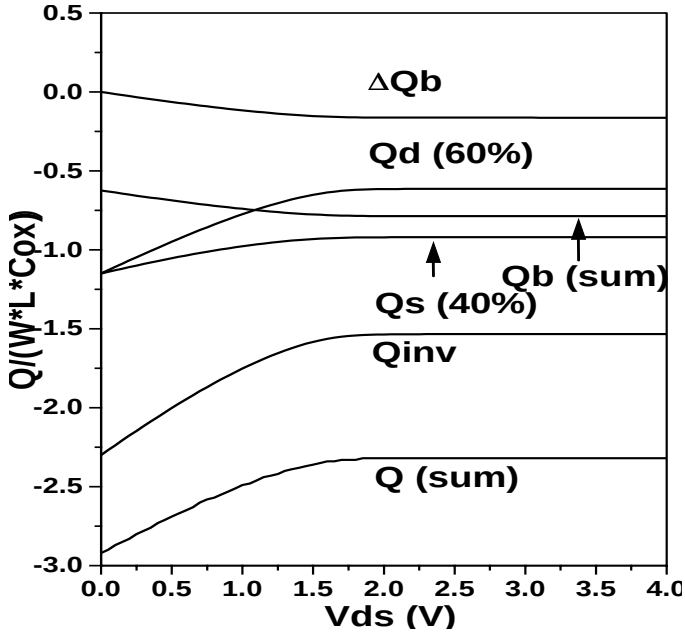

Figure 4-1. Normalized charge versus Vds bias.

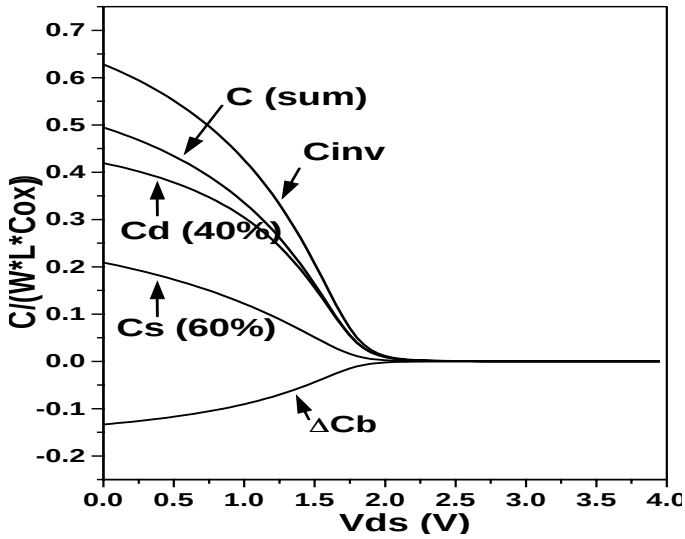

Figure 4-2. Normalized capacitance versus Vds bias.

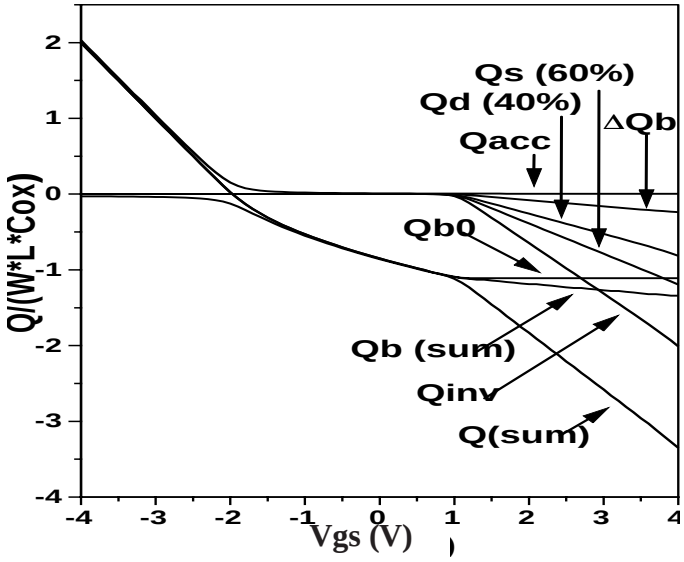

Figure 4-3. Normalized charge versus Vgs bias.

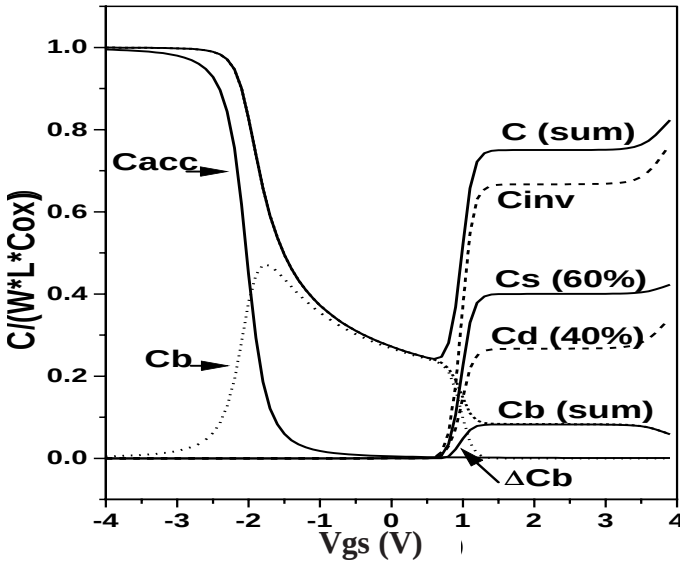

Figure 4-4. Normalized capacitance versus Vgs bias.

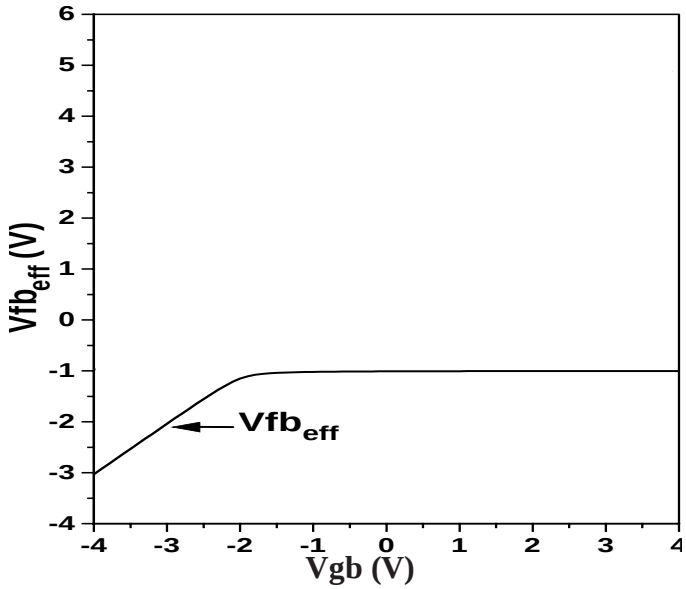

Figure 4-5. Continuity of the Vfbeff function.

